

**Amendments to the Specification:**

On page 1:

Please replace the paragraph beginning at line 9, with the following amended paragraph:

“High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with Improved Board-to-Board Interconnection Cable Length Identification System,” Serial No. 09/655,595, filed September 6, 2000\_\_\_\_\_, filed \_\_\_\_\_, (Attorney Docket No. ~~POU9-2000-0045-US1~~).

Please replace the paragraph beginning at line 13, with the following:

“High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with an Improved Maintenance Bus that Streams Data at High Speed,” Serial No. 09/656,147, filed September 6, 2000\_\_\_\_\_, filed \_\_\_\_\_, (Attorney Docket No. ~~POU9-2000-0046-US1~~).

Please replace the paragraph beginning at line 17, with the following:

“High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with a Method to Allow Memory Read/Writes Without Interrupting the Emulation,” Serial No. 09/655,596, filed September 6, 2000\_\_\_\_\_, filed \_\_\_\_\_, (Attorney Docket No. ~~POU9-2000-0048-US1~~).

Please replace the paragraph beginning at line 21, with the following:

“High Speed Software Driven Emulator Comprised of a Plurality of Emulation Processors with Improved Multiplexed Data Memory,” Serial No. 09/656,146, filed September 6, 2000\_\_\_\_\_, filed \_\_\_\_\_, (Attorney Docket No. ~~POU9-1999-0183-US1~~).

On page 7:

Please replace the paragraph beginning at line 5, with the following:

Briefly, this invention contemplates the provision of a system and method for bulk transfer to and from the SRAMs in which a starting memory address is latched and is then incremented every clock cycle to generate a new memory address, as described more extensively in copending application Serial No. 09/655,596 filed September 6, 2000\_\_\_\_\_, filed \_\_\_\_\_.

\_\_\_\_\_ and assigned to the assignee of this application. The addresses are decoded and memory requests are pipelined to the SRAM memory, one every clock cycle. When the memory controller detects transfer of the boundary of a predetermined number of clock cycles or words (e.g. 64 words or four clock cycles) the burst mode of data transfer is stopped and the memory controller waits for a “done” signal before resuming another cycle of the burst transfer mode. The memory controller on detecting a request on this address boundary first does a memory refresh followed by a requested operation; e.g. a continuation of the transfer operation.

On page 8:

Please replace the paragraph beginning at line 21, with the following amended paragraph:

For bulk transfers in accordance with the teachings of this invention, a latch is set by one of the ET4 control stores to inhibit further transfers between the ET4 processor chip and the SDRAMs on the module, as described in detail in copending application serial number 09/655,596, \_\_\_\_\_, (POU9-2000-0048-US1). The memory controller 22 includes incrementing logic into which a starting SDRAM address is inserted when the emulator is to perform a bulk data transfer operation. This memory address is ~~isn~~ incremented by “1” in response to each clock signal. Similarly,